FOUNDER

eMMC

MKEV016GIB-OY500

Specification

Advance

Revision 1.0

May 22, 2018

Foreword

This specification is subject to change without notice.MKEV016GIB-OY500 MFGR has the right to make changes to improve functions. Although the information in this document has been carefully reviewed,MKEV016GIB-OY500 MFGR assumes no responsibility for any errors contained herein and does not assume any liability arising out of the use of the product or circuit described herein.

Statement of Scope

This datasheet document is described the eMMC MKEV016GIB-OY500 of methods and abstractions of reliability. The contents include the concept and measurement methodologies.

Revision History

Revision	Date	Modified By	Description
1.0	2018/5/22	Angel xu	Initial release

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1. Product List

Capacity	eMMC P/N	NAND Type	User Density	Package Size	Pin
16GB	MKEV016GIB-OY500	128Gb x 1	91.53%	11.5mmx13mmx1.0mm	153 FBGA

2. Key Features

- Compatible to JEDEC Embedded Multi-Media Card (eMMC) Electrical Standard (5.0)
- Data bus width: 1bit(Default), 4bit and 8bit
- Not support large sector size (4KB)
- Interface power: V_{CCQ} (1.70V~1.95V or 2.7V~3.6V), Memory power: Vcc(2.7V~3.6V)
- Temperature: Operation (-25℃~85℃), storage (-40℃~85℃)
- User Density:

eMMC P/N	Density	LBA(Hex)	LBA(Dec)	Capacity(Bytes)
MKEV016GIB-OY500	16GB	0x1D49FFF	30,711,807	15,724,445,696

3. Pin Configuration

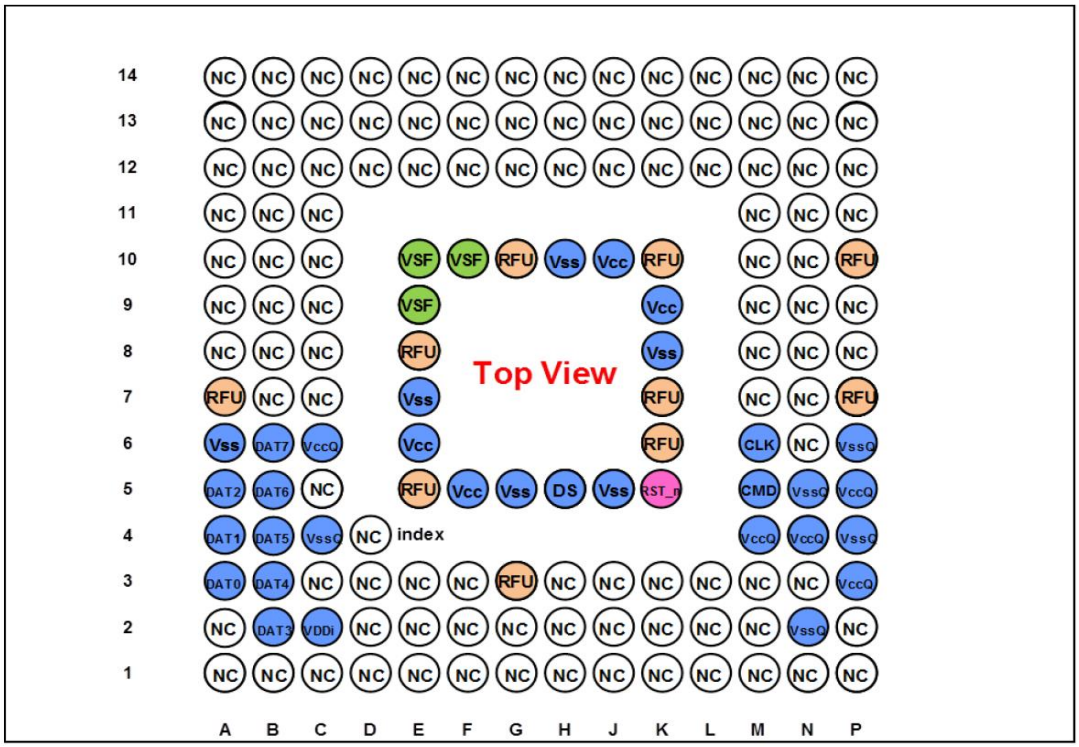


Figure 1 153 FBGA

[Table 1] 153 Ball Information

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A3	DAT0	C2	VDDi	J5	Vss	N4	VccQ
A4	DAT1	C4	VssQ	J10	Vcc	N5	VssQ
A5	DAT2	C6	VccQ	K5	RST_n	P3	VccQ
A6	Vss	E6	Vcc	K8	Vss	P4	VssQ
B2	DAT3	E7	Vss	K9	Vcc	P5	VccQ
B3	DAT4	F5	Vcc	M4	VccQ	P6	VssQ
B4	DAT5	G5	Vss	M5	CMD		

B5	DAT6	H5	DS	M6	CLK		
B6	DAT7	H10	Vss	N2	VssQ		

4. Package Information

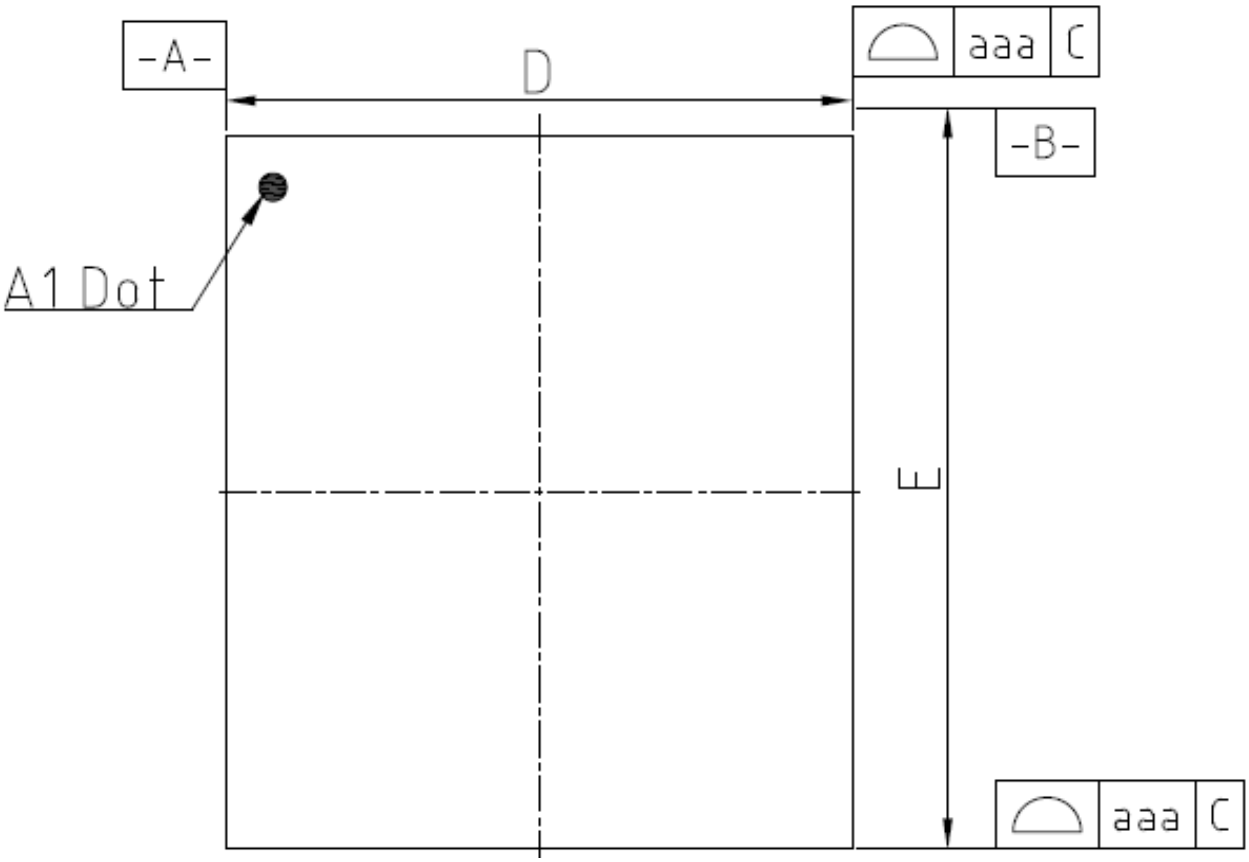


Figure 2 TOP View of Package

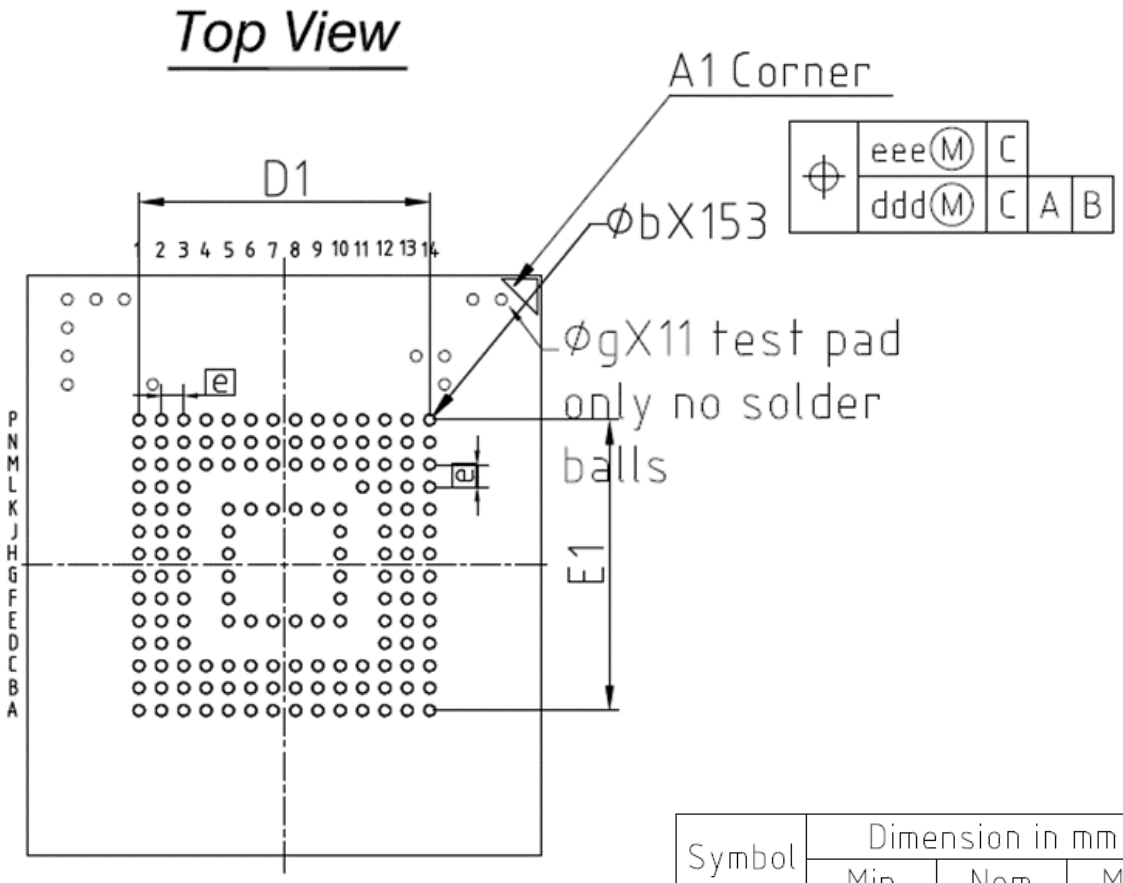


Figure 3 Bottom View of Package

Symbol	Dimension in mm		
	Min	Nom	Max
A	---	---	1.1
A1	0.16	0.21	0.26
A2	0.61	0.63	0.64
c	0.15	0.17	0.19
ϕg		0.25	
ϕb	0.25	0.30	0.35
D	11.40	11.50	11.60
D1	---	6.50	---
E	12.90	13.00	13.10
E1	---	6.50	---
e	0.50 BSC		
aaa	0.15		
bbb	0.20		
ccc	0.20		
ddd	0.15		
eee	0.10		
MD/ME	14/14		

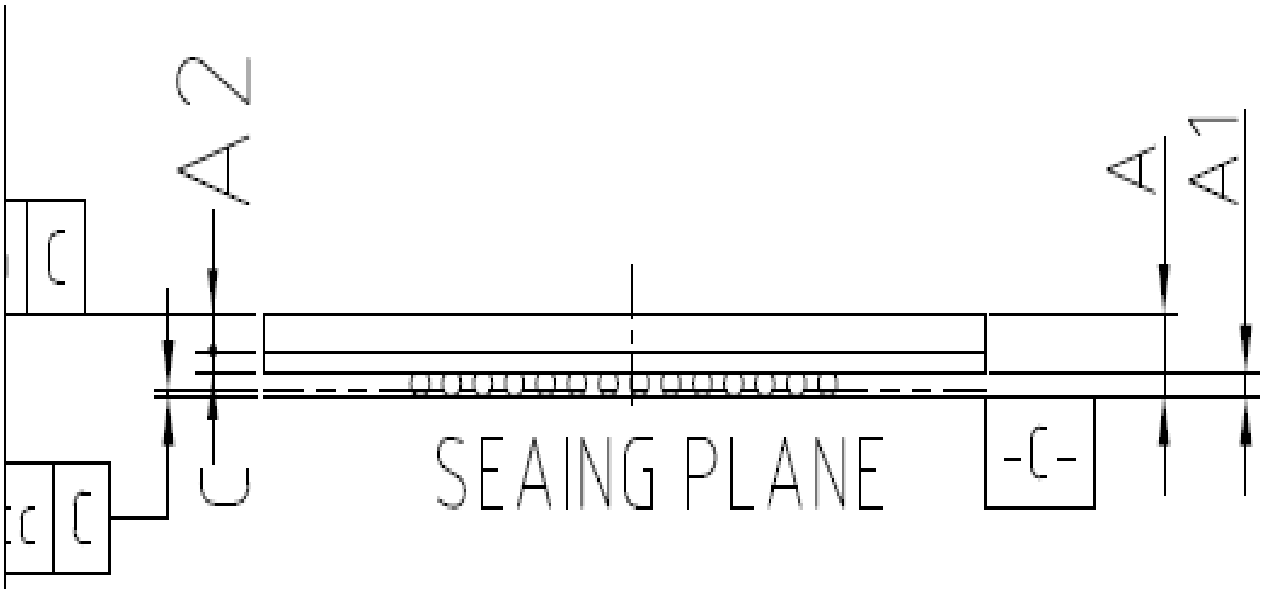


Figure 4 Side View of Package

5. eMMC Register Value

5.1 OCR Register

[Table 2] OCR Register

OCR bit	VDD voltage window	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 – 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)
[31]	eMMC power up status bit	

5.2 CID Register

[Table 3] CID Register

Name	Field	Width	CID-slice	CID Value
Manufacture ID	MID	8	[127:120]	0xEA
Reserved		6	[119:114]	---
Card/BGA	CBX	2	[113:112]	0x01
OEM/Application ID	OID	8	[111:104]	0x0E
Product name	PNM	48	[103:56]	16GB: 911000(0x39313130303030)
Product revision	PRV	8	[55:48]	0x10

Product serial number	PSN	32	[47:16]	0x1
Manufacture date	MDT	8	[15:8]	0x5
CRC7 checksum	CRC	7	[7:1]	---
not used, always '1'	-	1	[0:0]	0x1

5.3 CSD Register

[Table 4]CSD Register

Name	Field	Width	Cell Type	CSD-slice	CID Value
CSD Structure	CSD-STRUCTURE	2	R	[127:126]	0x03
System specification version	SPEC_VERS	4	R	[125:122]	0x04
Reserved	-	2	R	[121:120]	-
Data read access-time 1	TAAC	8	R	[119:112]	0x27
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x00
Max.bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Device command classes	CCC	12	R	[95:84]	0xF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00
DSR implemented	DSR_IMP	1	R	[76:76]	0x00

Reserved	-	2	R	[75:74]	-
Device size	C_SIZE	12	R	[73:62]	0xFFF
Max. read current@VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x07
Max. read current@VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x07
Max. write current@VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x07
Max. write current@VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x07
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write Protect group size	WP_GRP_SIZE	5	R	[36:32]	0x07
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01
Manufacture default ECC	DEFAULT_ECC	2	R	[30:29]	0x00
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x04
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00
Reserved	-	4	R	[20:17]	-
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00
Copy flag(OTP)	COPY	1	R/W	[14:14]	0x00

Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00
File Format	FILE_FORMAT	2	R/W	[11:10]	0x00
ECC code	ECC	2	R/W/E	[9:8]	0x00
CRC	CRC	7	R/W/E	[7:1]	0x25
Not used, always '1'	-	1	-	[0:0]	0x1

5.4 Extended CSD Register

[Table 5] Extended CSD Register

Name	Field	Size	Cell Type	CSD-slice	CSD Value
Reserved[1]		6	-	[511:506]	-
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x0
Supported Command Sets	S_CMD_SET	1	R	[504]	0x1
HPI features	HPI_FEATURES	1	R	[503]	0x1
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x0
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x5
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x5
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	0x0
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0x0

Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0x0
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x0
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x0
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x0
Supported modes	SUPPORTED_MODES	1	R	[493]	0x1
FFU features	FFU_FEATURES	1	R	[492]	0x1
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x10
FFU Argument	FFU_ARG	4	R	[490:487]	0xFEF00000
Reserved[1]		181	TBD	[486:306]	0x0
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0x0
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	0x0
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x1
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x1
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x0
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x4
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x4
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x4

Device version	DEVICE_VERSION	2	R	[263:262]	0x517
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	0x0000024416080517
Power class for 200MHz, DDR at VCC= 3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x0
Cache size	CACHE_SIZE	4	R	[252:249]	0x0
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x5
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C
Background operations status	BKOPS_STATUS	1	R	[246]	0x0
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x0
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0xA
Reserved[1]		1	-	[240]	-
Power class for 52MHz, DDR at V_{CC} = 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x55
Power class for 52MHz, DDR at V_{CC} = 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x55
Power class for 200MHz at V_{CCQ} =1.95V, V_{CC} = 3.6V	PWR_CL_200_195	1	R	[237]	0x55

Power class for 200MHz at V_{CCQ} =1.3V, V_{CC} = 3.6V	PWR_CL_200_130	1	R	[236]	0x0
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x0
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x0
Reserved		1	-	[233]	-
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x3
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x46
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x3C
Boot information	BOOT_INFO	1	R	[228]	0x7
Reserved		1	-	[227]	-
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	0x20
Access size	ACC_SIZE	1	R	[225]	16GB:07
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x1
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x1

Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x1
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	16GB:08
Sleep current (VCC)	S_C_VCC	1	R	[220]	0x8
Sleep current (VCCQ)	S_C_VCCQ	1	R	[219]	0x7
Production state awareness time out	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0xA
Sleep/awake time out	S_A_TIMEOUT	1	R	[217]	0x13
Sleep Notification Tim out[1]	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x10
Sector Count	SEC_COUNT	4	R	[215:212]	16GB:0x1D4A000
Reserved	-	1	-	[211]	-
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x8
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0x8
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x8
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x8

Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x8
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0x8
Reserved		1	-	[204]	-
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x7
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x7
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x7
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x7
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x5
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x19
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	0x1F
Device type	DEVICE_TYPE		R	[196]	0x57
Reserved1		1	-	[195]	_
CSD STRUCTURE	CSD_STRUCTURE	1	R	[194]	0x2
Reserved[1]		1	TBD	[193]	-
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x7
Modes Segment					
Command set	CMD_SET	1	R/W/E_P	[191]	0x0

Reserved[1]		1	TBD	[190]	_
Command set revision	CMD_SET_REV	1	R	[189]	0x0
Reserved[1]		1	TBD	[188]	_
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x0
Reserved[1]		1	TBD	[186]	_
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x0
Reserved[1]		1	TBD	[184]	_
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x0
Reserved[1]		1	TBD	[182]	_
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x0
Reserved[1]		1	TBD	[180]	_
Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0x0
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	[178]	0x0
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x0
Reserved[1]		1	TBD	[176]	_
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x0
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x0
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x0

Reserved[1]		1	TBD	[172]	_
User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	[171]	0x0
Reserved[1]		1	TBD	[170]	_
FW configuration	FW_CONFIG	1	R/W	[169]	0x0
RPMB Size	RPMB_SIZE_MULT		R	[168]	0x20
Write reliability setting register	WR_REL_SET		R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM		R	[166]	0x5
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x0
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x0
Enable background operations handshake	BKOPS_EN		R/W	[163]	0x0
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x0
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x0
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	0x3
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x0F2A5
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x0
Partitioning Setting	PARTITION_SETTING_ COMPLETED	1	R/W	[155]	0x0

General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x0
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x0
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x0
Reserved[1]		1	TBD	[135]	-
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x0
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x0
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x0
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x0
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x0
Reserved[1]	-	2	-	[129:128]	-
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	vendor specific	[127:64]	0x0
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x0
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x0
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x0
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0xA

Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x0
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0x0
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x0
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x0
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x0
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x0
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x0
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x0
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x0
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x0
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x0
Reserved[1]		1	TBD	[31]	0x0
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x0
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x0
Reserved[1]		1	TBD	[28:27]	0x0
FFU status	FFU_STATUS	1	R	[26]	0x0

Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x0
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	16GB: 0x0E0F0A3
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	0x3
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x0
Reserved[1]	-	16	-	[15:0]	-

6. eMMC AC Parameter

6.1 Timing Parameter

Timing Parameter		Max. Value	Unit
Initialization Time(tINIT)	Normal	1	s
	After partition setting	1	s
Read Time out		100	ms
Write Time out		250	ms
Erase Time out		100	ms
Force Erase Time out		3	Min
Secure Erase Time out		22	s
Secure Trim step1 Time out		5	s
Secure Trim step2 Time out		17	s
Trim Time out		900	ms
Partition Switching Time out (after Init)		1.6	ms

Power Off Notification(short) Time out		100	ms
Power Off Notification(long) Time out		600	ms

6.2 Bus Timing Specification in HS400 mode

6.2.1 HS400 Device Input Timing

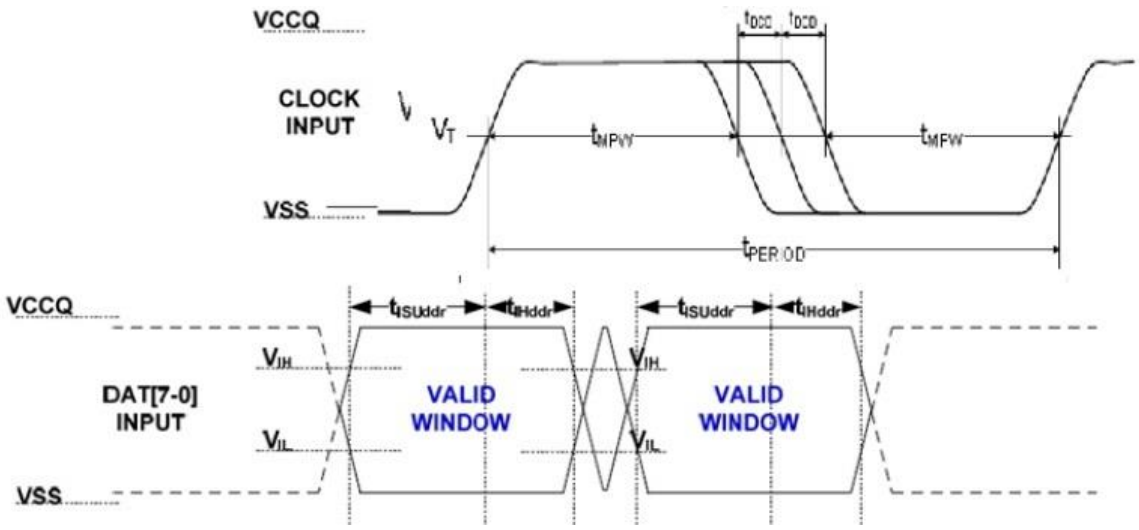


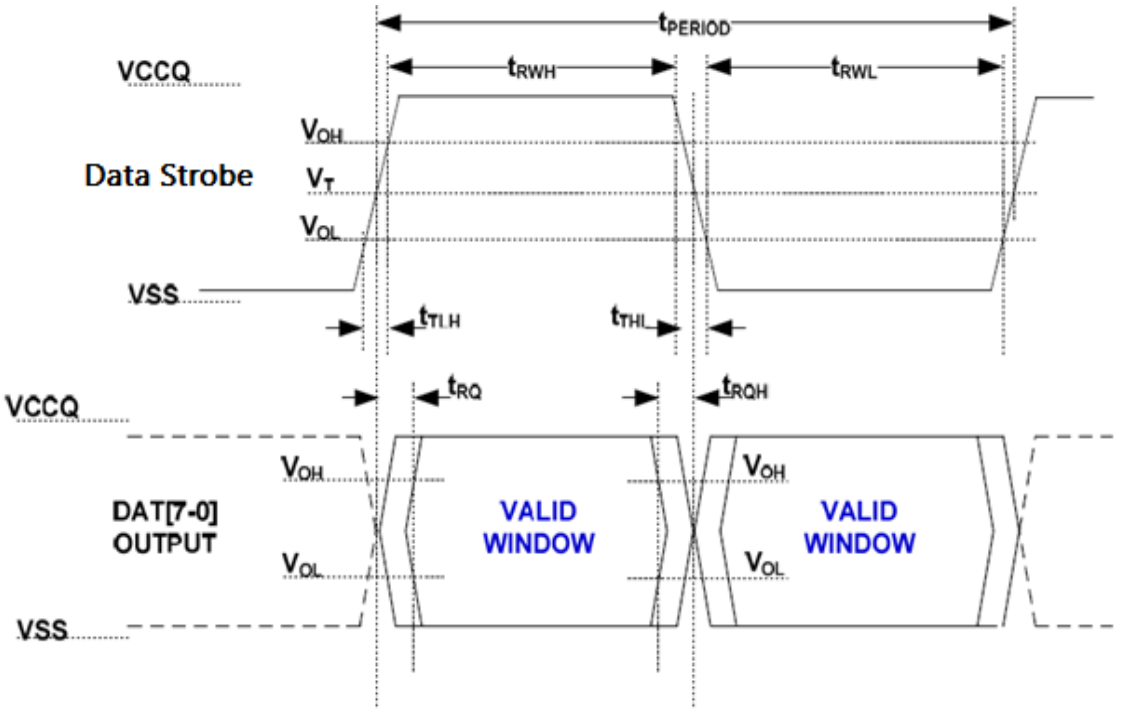
Figure 5 HS400 Device Input Timing

[Table 6] HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5			200MHz(Max), between rising edges With respect to V_T.
Slew rate	SR	-1.125		V/ns	With respect to V_T
Duty cycle distortion	tCKDCD	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T.

					Includes jitter, phase noise
Minimum pulse width	tCKMPW	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input set-up time	tISUddr	0.4		ns	$C_{Device} \leq 6pF$ With respect to V_{IH}/V_{IL}.
Input hold time	tIHddr	0.4		ns	$C_{Device} \leq 6pF$ With respect to V_{IH}/V_{IL}.
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}.

6.2.2 HS400 Device Output Timing



Note: V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

Figure 6 HS400 Device Output Timing

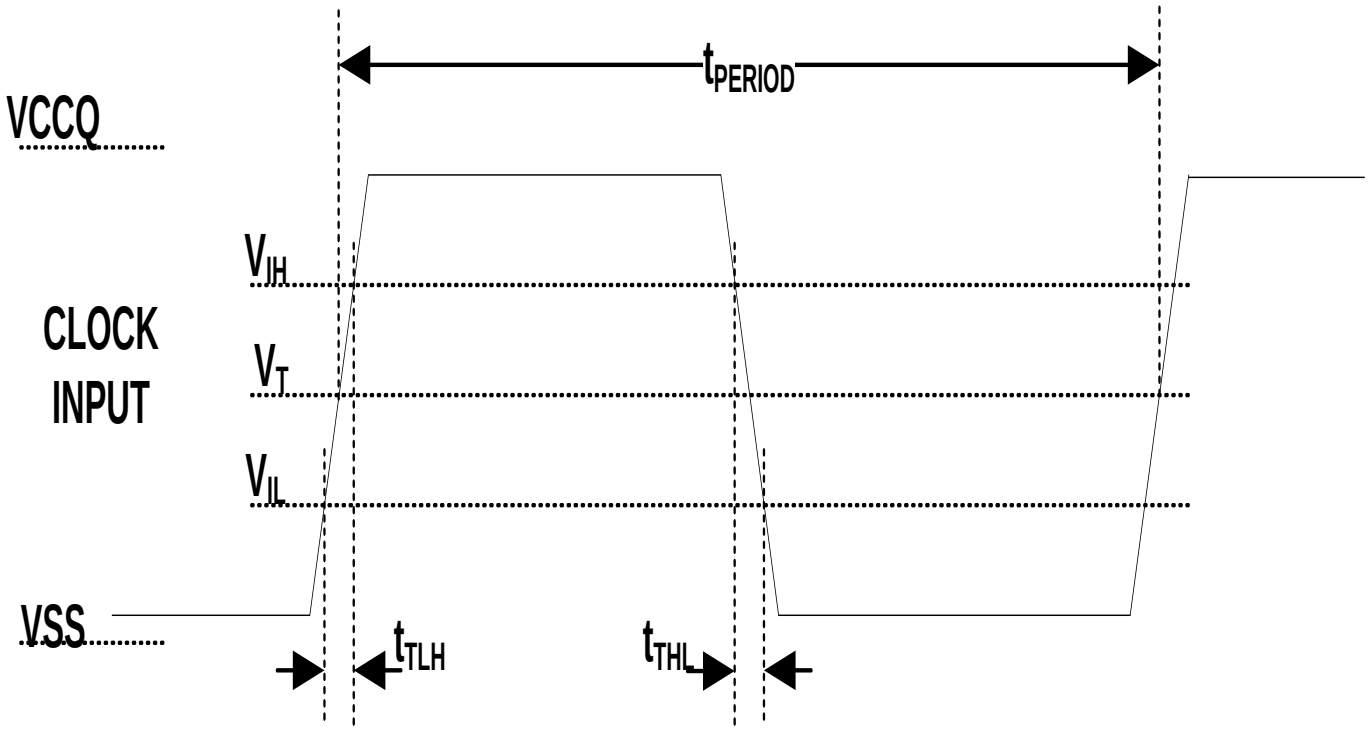
[Table 7] HS400 Device Output Timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5			200MHz(Max), between rising edges With respect to V_T
Slew rate	SR	-1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK timing. With respect to V_T Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.0		ns	With respect to V_T
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid
Read post-amble	t_{RPST}	0.4	-	t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid

Output DAT (referenced to Data Strobe)					
Output skew	tRQ		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	tRQH		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load.
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

6.3 Bus Timing Specification in HS200 mode

6.3.1 HS200 Device Clock Timing



Note1: V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

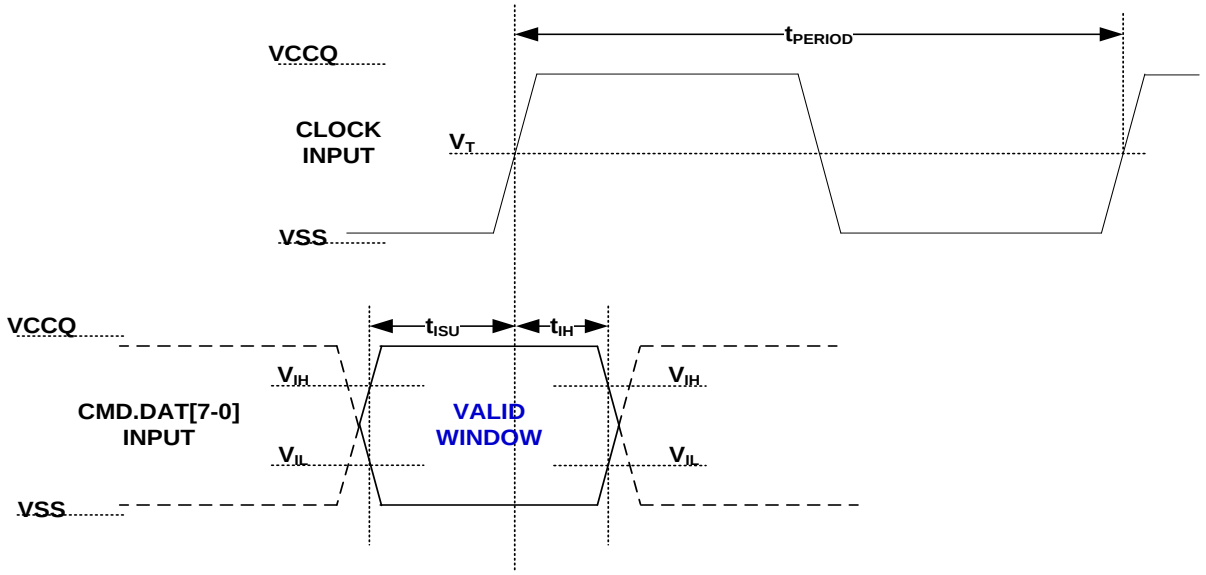
Note2: V_T=0.975V - Clock Threshold (V_{CCQ} = 1.8V) and V_T=0.65V - Clock Threshold (V_{CCQ} = 1.2V) , indicates clock reference point for timing measurements.

Figure 7 HS200 Device Clock Timing

[Table 8] HS200 Device Clock Timing

Symbol	Min.	Max.	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	0.2· t_{PERIOD}	ns	tTLH, tTHL < 1ns (max.) at 200MHz, C_{DEVICE}=6pF, The absolute maximum value of tTLH, tTHL is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

6.3.2 HS200 Device Input Timing



Note1: t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).

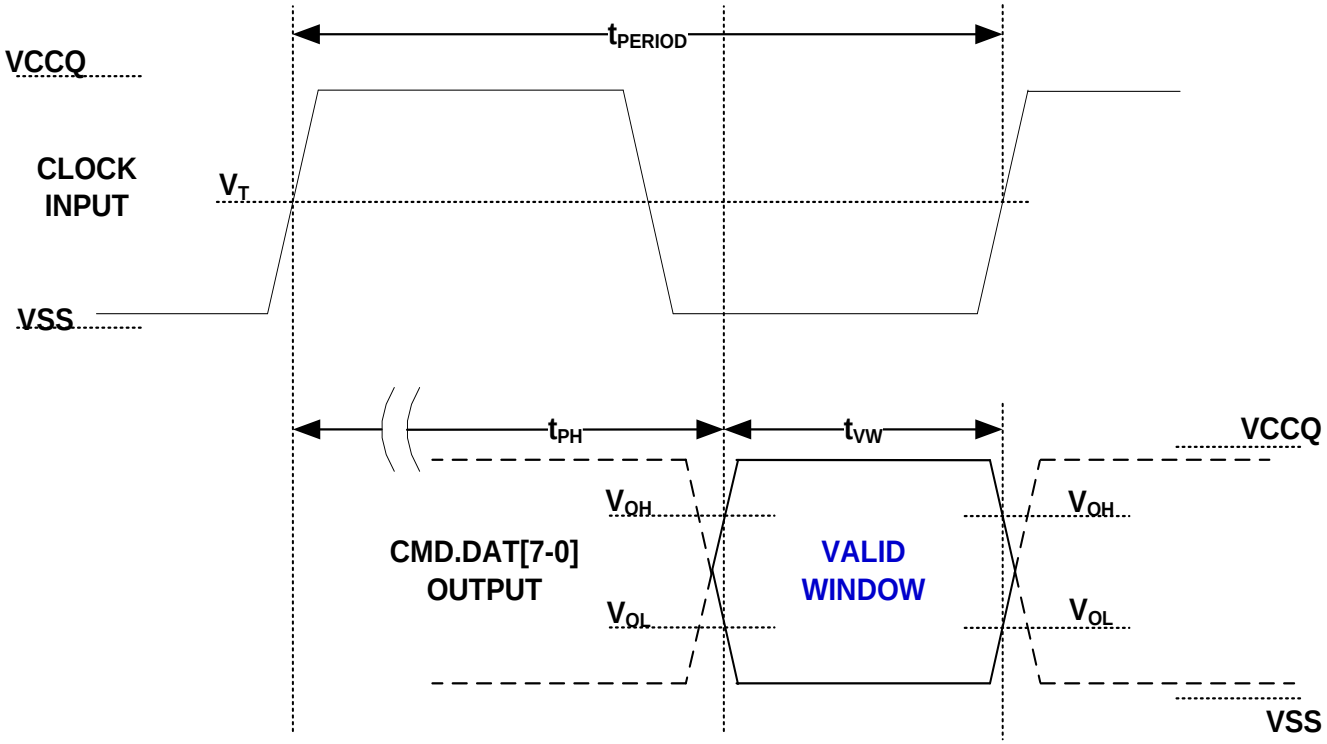
Note2: V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 8 HS200 Device Input Timing

[Table 9] HS200 Device Input Timing

Symbol	Min.	Max.	Unit	Remark
t_{ISU}	1.40	-	ns	C_{DEVICE} ≤6pF
t_{IH}	0.8		ns	C_{DEVICE} ≤6pF

6.3.3 HS200 Device Output Timing



Note: V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

Figure 9 HS200 Device Output Timing

[Table 10] HS200 Device Output Timing

Symbol	Min.	Max.	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output.

				Does not include a long term temperature drift.
Δ_{TPH}	-350 (ΔT= -20℃)	+1550 (ΔT=90℃)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure Δ_{TPH} is 2600ps for ΔT from -25℃ to 125℃ during operation.
t_{VW}	0.575	-	UI	t_{VW}=2.88ns at 200MHz Using test circuit in Figure 6 including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected T_{VW} at Host input is larger than 0.475UI.

Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.

eMMC DC Parameter

6.4 Supply Voltage

[Table 11] Supply voltage

Item	Min	Max	Unit
V_{CCQ}	1.70(2.7)	1.95(3.6)	V
Vcc	2.7	3.6	V
Vss	-0.5	0.5	V

6.5 Bus Signal Line Load

[Table 12] Bus Signal Line Load

Paramter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistence for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floaing
Pull-up resistence for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistence DAT1-DAT7	Rint	10		150	KOhm	to prevent unconnected lines floating
Single e · MMC capacitance	C_{BGA}			12	pF	
Maximum single line inductance				16	nH	Fpp<=52MHz

[Table 13] Capacitance and Resistance for HS400 mode

Paramter	Symbol	Min	Typ.	Max	Unit	Remark
Bus signal line capacitance	CL			13	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	

Pull-down resistance for Data Strobe	$R_{Data\ Strobe}$	10		100	Kohm	